Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-17. (Canceled)

18. (Currently Amended) Method of addressing an array of microsystems which can be individually addressed by a control circuit, the control circuit and each microsystem including an electromagnetic transmission means, and each microsystem further including a counter, a register, and a read-only memory containing an identification code, the method comprising:

an initialization phase, where the control circuit successively addresses the microsystems by their respective identification codes and stores a reduced addressing code in the respective registers of the microsystems; and

an addressing phase, where the control circuit transmits successive increment signals, and where the microsystems ~~monitor~~ control resetting of their respective counters and, upon receipt of an increment signal, the microsystems increment a content of their respective counters and compare the content and their respective reduced addressing code, so as to trigger execution of a pre-determined command when the content of the counter and the reduced addressing code are identical.

19. (Previously Presented) Method of addressing the array of microsystems according to claim 18, wherein the respective reduced addressing code of a microsystem is a function of its position in the array.

20. (Previously Presented) Method of addressing the array of microsystems according to claim 18, wherein the reduced addressing codes of the microsystems correspond to increasing numbers.

21. (Currently Amended) Method of addressing the array of microsystems according to claim 18, wherein the microsystems are arranged in lines and columns, the respective reduced addressing code of each microsystem comprising a line number and a column number respectively stored in line and column registers of the microsystem, contents of the line and column registers being respectively compared with the contents of ~~the line~~ line and column counters of the microsystems.

22. (Previously Presented) Method of addressing the array of microsystems according to claim 21, wherein the control circuit successively transmits line increment signals and column increment signals, the line increment signals causing the contents of the line counters to be incremented and the column increment signals causing the contents of the column counters to be incremented and the line counters to be reset.

23. (Previously Presented) Method of addressing the array of microsystems according to claim 22, wherein the microsystems are arranged in lines, in columns and according to height, the respective reduced addressing code of each microsystem comprising an additional number associated to the height, stored in an additional register associated to the height, each microsystem comprising an additional counter associated to the height, contents of the register associated to the height being compared with the contents of the counter associated to the height.

24. (Previously Presented) Method of addressing the array of microsystems according to claim 23, wherein the control circuit transmits height increment signals causing the additional counters associated to the height to be incremented and the line and column counters of all the microsystems to be reset.

25. (Previously Presented) Method of addressing the array of microsystems according to claim 18, wherein a microsystem transmits an acquit signal after the execution of the command by the microsystem.

26. (Previously Presented) Method of addressing the array of microsystems according to claim 18, wherein the control circuit transmits data representative of a type of command to be executed by the microsystems in association with transmission of a reset signal.

27. (Previously Presented) Method of addressing the array of microsystems according to claim 18, wherein the control circuit transmits data representative of a type of command to be executed by the microsystems in association with transmission of an increment signal.